AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A data processor comprising:

a CPU;

an internal memory accessible by said CPU; and

a control circuit capable of responding to a particular access request issued by said CPU to control a block transfer, in which said internal memory is used as ~~one~~ a first transfer object,

wherein a set of instructions for said CPU includes a particular instruction for making said CPU issue the particular access request,

the particular instruction has an addressing field, and

when an address specified by the addressing field coincides with ~~an~~ a logical address mapped to said internal memory, the address is set as one of a transfer source address or a~~and~~ transfer destination address~~addresses~~ of the block transfer, and

a complementary~~the other of the~~ transfer source address or~~and~~ transfer destination address~~es~~ of the block transfer

is a physical address corresponding to a different logical address~~held by the addressing field~~, and is associated with a second transfer object.

Claims 2-4 (canceled)

5. (currently amended) The data processor of Claim ~~2~~1, further comprising a bus interface controller connected to said control circuit,

wherein said bus interface controller is capable of performing interface control of the ~~other~~ second transfer object.

6. (currently amended) The data processor of Claim 1, further comprising a cache memory,

wherein said cache memory shares a first bus with said CPU, said internal memory, and said control circuit.

7. (original) The data processor of Claim 6, wherein said internal memory is assigned a cache non-object address for said cache memory.

8. (currently amended) The data processor of Claim 7, further comprising a second bus used exclusively for connecting said control circuit with said internal memory,

wherein said second bus can be utilized for a data block transfer in response to the particular access request.

9. (currently amended) The data processor of Claim 8, wherein said control circuit is capable of performing memory control in regard to a cache hit and a cache miss with respect to said cache memory.

10. (currently amended) The data processor of Claim 7, wherein the ~~set of instructions for said CPU~~ particular instruction includes a first cache memory-operating instruction, and

~~the first cache memory-operating instruction causes an operation of making said cache memory retain data at a cache object address specified by the addressing field~~ when the logical address specified by the addressing field directs a cache object address for said cache memory, the first cache memory-operating instruction causes an operation of making said cache memory retain data of an external memory associated with the physical address corresponding to the

different logical address, at a cache object address specified by the logical address.

11. (currently amended) The data processor of Claim ~~7~~10, wherein the ~~set of instructions for said CPU~~ particular instruction includes a second cache memory-operating instruction, and

when ~~a cache hit is detected at a cache object address specified by the addressing field~~ the logical address specified by the addressing field directs a cache object address and a cache hit is detected at a data location specified by the logical address and a cache entry associated with the cache hit is dirty, the second cache memory-operating instruction causes an operation of writing back ~~the cache entry~~ to the external memory.

12. (currently amended) The data processor of Claim 10, wherein the particular instruction has an operation code identical ~~with~~ to that of the first cache memory-operating instruction, and sets the cache non-object address of the addressing field as the destination address.

13. (currently amended) The data processor of Claim 11, wherein the particular instruction has an operation code

identical ~~with~~ to that of the second cache memory-operating instruction, and sets the cache non-object address of the addressing field as the source address.

14. (original) The data processor of Claim 5, further comprising a data transfer control circuit connected with said bus interface controller.

15. (original) The data processor of Claim 14, further comprising an external interface circuit for connection of an external bus, which is connected with said bus interface controller.

Claims 16-20 (canceled)